

BU9-98-110DIV

09/666,325

- 1 15. (Amended) A semiconductor device having at least two levels of interconnecting
2 metallurgy, said semiconductor device comprising:
3 a first level of substantially silicide free metallurgy; and
4 an uppermost layer of metallurgy including a bonding pad, wherein a top of said
5 uppermost layer comprises a silicided surface,
6 wherein said uppermost layer maintains performance of said semiconductor device
7 irrespective of resistivity shifts.

- 1 21. (Amended) A semiconductor device comprising:
2 an exterior surface having a top level of metallurgy,
3 wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and
4 wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,
5 wherein said silicided surface maintains performance of said semiconductor device
6 irrespective of resistivity shifts.

- 1 29. (Amended) A semiconductor chip comprising:
2 an exterior surface having a top level of metallurgy; and
3 an interior having at least one internal level of metallurgy,
4 wherein said top level of metallurgy is thicker than said internal level of metallurgy,
5 wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and
6 wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,
7 wherein said silicided surface maintains performance of said semiconductor device
8 irrespective of resistivity shifts.